Total No. of Questions : 12]

SEAT No. :

P2007

[Total No. of Pages : 2

[5254]-178

B.E. (Computer Engineering)

VLSI & Digital System Design

(2008 Pattern) (Elective - IV) (Semester - II)

Time : 3 Hours] *[Max. Marks : 100*

Instructions to the candidates:

1) ***Answer Question No. 1 OR 2, 3 OR 4, and 5 OR 6 from Section - I and Q. No.7 OR 8,9 OR 10 and 11 OR 12 from Section - II.***
2) ***Answers to the two Sections must be written in separate answer books.***
3) ***Neat diagram must be drawn whenever necessary.***
4) ***Figures to the right indicate full marks.***
5) ***Assume suitable data, if necessary.***

SECTION - I

Q1) a) Compare Speed-Power performance of ECL, CMOS, BiCMOS. **[9]**

b) Explain types of technology scaling. **[8]**

OR

Q2) a) Explain layout design rules for devices and interconnects. **[9]**

b) Explain different tools for device simulation. **[8]**

Q3) a) Explain Shallow Trench Isolation (STI) with process flow. **[8]**

b) Explain fabrication process for CMOS device. **[9]**

OR

Q4) a) Explain fabrication of Cu interconnects with suitable diagram. **[8]**

b) Explain the different process options for device isolation. **[9]**

Q5) a) Explain basic properties of Silicon Wafer. **[4]**

b) Explain purification steps of raw- silicon wafer. **[4]**

c) Explain Chemical vapor oxidation technique. **[8]**

OR

Q6) a) Write a short note on **[8]**

i) Nano imprint lithography

ii) Electron-beam lithography

b) Explain the different techniques of etching **[8]**

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SECTION - II

Q7) a) Explain island style and Row based FPGA architectures in detail. **[8]**

b) Explain different Modelling styles in HDL. **[9]**

OR

Q8) a) Explain following terms with examples **[9]**

i) Identifier

ii) Variable

iii) Array

b) Write VHDL Code for Lift controller. **[8]**

Q9) a) Explain the types of programmable logic devices in detail. **[8]**

b) Explain Application Specific IC's Design flow. **[4]**

c) Explain CMOS inverter with VTC. **[4]**

OR

Q10)a) Explain static and dynamic behaviour of CMOS devices and circuits. **[8]**

b) Explain role of software tools in digital design. Explain the types of software tools in VLSI design. **[8]**

Q11)a) Explain the metastability in detail. **[5]**

b) List out different steps for designing clocked synchronous machine. **[8]**

c) Explain merits and demerits of CPLD. **[4]**

OR

Q12)a) Explain timing parameters for read and write operation in static RAM. **[8]**

b) For combinational logic explain the following **[9]**

i) Timing diagram

ii) Propagation delay

iii) Timing specification